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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,786	12/04/2003	Duck Young Jung	SUN0034US	6887

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EXAMINER	
PETERSON, CHRISTOPHER K	
ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
09/30/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/727,786	JUNG, DUCK YOUNG	
	Examiner	Art Unit	
	CHRISTOPHER K. PETERSON	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 7/23/2009 have been fully considered but they are not persuasive.

First, in regard to claims 1 and 5, the Applicant argues the Pettinelli reference (US Patent # 6,254,003) does not teach “a second A/D converter for directly receiving the output signals of the image sensor and converting the received output signals into digital signals, wherein the shutter control signal is generated by using the output signals of the second A/D converter" (See Remarks, Pg. 5 - 7). The Examiner respectfully disagrees. Specifically, noting the Pettinelli reference, Fig. 1, 3, 3A, 4B , 5A and Col. 6, lines 17 – 29 and Col. 6, lines 51 – 63, Col. 8, lines 38 – 59, and Col. 10, lines 15 - 57 shows the “a second A/D converter for directly receiving the output signals of the image sensor and converting the received output signals into digital signals, wherein the shutter control signal is generated by using the output signals of the second A/D converter". Applicant argues Pettinelli uses an A/D converter as a means for determining a window state, not for generating a shutter control signal SSC. Applicant also highlights Column 8, lines 38 and 39 “the analog output signal of sensor 30 is converted to digital form by the **external A/D converter or by an A/D converter (second A/D converter)** that is built into processor 60. Once converted to digital form, the illumination signal (conductor 95) may be processed by means of a digital window detecting subroutine to produce window state

signals, such as those shown in Table 1. Examiner respectfully disagrees that Pettinelli uses an A/D converter as a means for determining a window state, not for generating a shutter control signal SSC. Pettinelli (Fig. 2) teaches a window detector circuit (90) includes a first and second comparator to provide the control microprocessor (60) a Max and Min reference level for the illumination signal (conductor 95) (Col. 8, lines 5 – 30). Pettinelli (Fig. 4B) teaches the start of a scan directs the processor to a set of blocks 130, 135, 140, 145 and 150, which together sample the illumination signal (conductor 95), and determine if it has a magnitude that is within a predetermined window of acceptable illumination values. These steps are accomplished by examining the outputs of window detector 90 to determine which of the states shown in Table 1 applies (Col. 10, lines 25 - 46). The control microprocessor (60) first encounters a block 190 which directs it either to block 192 or 194, depending on whether the "too bright" or the "too dark" flag has been set. If it is the former, the stored shutter count value is incremented by 1 to reduce the exposure time by one unit; if it is the latter, the shutter count is decremented by one to increase the exposure time by one unit. In either case, the processor is directed to block 196, which causes it to set the updated shutter count into the working counter and clear the flags in preparation for the next scan (Col. 11, lines 35 -48). Pettinelli does teach the shutter control signal (exposure time) is generated by using the output signals of the second A/D converter (external A/D converter or by an A/D converter (second A/D converter) that is built into processor 60). For the above reasons, the

Examiner believes the Pettinelli reference does teach the limitations of claims 1 and 5, and the rejection to the claim will be set forth below.

Secondly, in regard to claims 1 and 5, the Applicant argues the Matsushima (US Patent Pub. # 2003/0016299) in view of Okino (US Patent # 5,371,539) and further in view of Pettinelli (US Patent # 6,254,003) do not teach “two A/D converters" (See Remarks, Pg. 7). The Examiner respectfully disagrees. Specifically, noting the Pettinelli reference, Fig. 1 and Col. 6, lines 4 - 16 shows the “two A/D converters". Applicant argues Matsushima, Okino, and Pettinelli teach only one A/D converter. Examiner respectfully disagrees. Pettinelli teaches the image sensor 30 serves to convert this optical image into an electrical output signal OS which is further processed by a signal processing circuit 45 and a comparator 50 to produce a digital output signal labeled DATA for application to a decoder (not shown) via output 20 (Col. 6, lines 4 – 16). Examiner analyzes this as the signal processing and comparator produce a digital signal for further processing by the output circuit (20) as cited by the Matsushima and Okino references and the second A/D converter is used to provide a shutter control signal (IGS and SH) to the image sensor. For the above reasons, the Examiner believes the Matsushima, Okino, and Pettinelli references do teach the limitations of claims 1 and 5, and the rejection to the claim will be set forth below.

Thirdly, in regard to claims 3, 4, 7, and 8, these claims depend on rejected independent claims 1 and 5. Therefore claims 3, 4, 7, and 8 are rejected as cited above in regards to independent claims 1 and 5.

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima (US Patent Pub. # 2003/0016299) in view of Okino (US Patent # 5,371,539) and further in view of Pettinelli (US Patent # 6,254,003).

As to claim 1, Matsushima (Fig. 2) teaches an image signal processing system comprising:

- an image sensor (CCD 6) for receiving an image of a subject in a light form under the control of a shutter control signal (digital shutter value) to generate analog signals (Para 56). Matsushima teaches the digital shutter value for the CCD (6) is determined by the signal processing circuit (10) (Para 56)
- a variable gain amplifier (automatic gain control circuitry (AGC) 8) for amplifying output signals of the image sensor (CCD 6) under the control of a gain control signal to maximize dispersion of the analog signals (Para 56).
- a first A/D converter (A/D 9) for receiving the output signals of the variable gain amplifier (8) and converting the received output signals into digital signals (Para 29 and 30);

- an image data processor (video signal processing circuit 10 and microcomputer 16) for receiving the output signals of the first A/D converter (9) and generating the gain control signal (variable control of AGC) and providing the generated shutter control signal (digital shutter value) to the image sensor (6) (Para 29 - 33 and 56). Matsushima teaches the video processing circuit 10 are switched by exchanging data with the microcomputer 16, and the circuit 10 can output exposure information, focus information, white balance information, and auto-focus information of a CCD signal to the microcomputer 16 as needed (Para 33 and 34).
- wherein the gain control signal are generated by using the output signals of the first A/D converter (9) (Para 29).

Matsushima does not teach a movement value, a second A/D converter, or the shutter control signal is generated by the output signals of the second A/D converter. Okino teaches a motion detecting circuit which receives the digital video signal calculates correlative values for each of a plurality of blocks constituting a whole screen according to a representative point matching method. A microcomputer calculates motion vectors of respective blocks on the basis of correlative value data from the motion detecting circuit and an average motion vector thereof, and calculates "increase", "passing degree" and "variation". Okino (Fig. 1) teaches an image data processor (microcomputer 26) for receiving the output signals of the first A/D converter (18) to find a movement value (positional and correlative values data) (Col. 4, lines 40 – 54). Therefore, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a motion detecting circuit as taught by Okino to the image sensing apparatus of Matsushima, because a picture stabilization with accuracy can be implemented and unintentional movement of a picture or image can be effectively prevented (Col. 2, lines 30 – 63 of Okino).

Matsushima in view of Okino do not teach a second A/D converter or the shutter control signal is generated by the output signals of the second A/D converter. Pettinelli reference teaches an exposure control circuitry uses the output of the window detecting circuit to control which of a plurality of the subdivisions of the exposure control range of the image sensor will be used. Changes in exposure time are made only between adjacent subdivisions of the exposure control range. Together with a predetermined hysteresis between the exit and re-entry thresholds of the window, the latter changes stabilize the operation of the reader by reducing exposure control "hunting" (Abstract). Pettinelli (Fig. 1) teaches an image data processor (control microprocessor 60) for receiving the output signals of the second A/D converter (A/D built into the control microprocessor 60) the shutter control signal (SH), and providing the generated shutter control signal to the image sensor (image sensor 30) (Col. 8, lines 38 – 59). Pettinelli further teaches the control microprocessor (60) controls the image sensor (30) via control signals (integration clear signal ICG and shift signal SH) (Col. 6, lines 17 – 29 and Col. 6, lines 51 – 63). The IGC signal is used to clear the image sensor output and functions as an electrical shutter. Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to have provided an A/D with shutter control circuit as taught by Pettinelli to the image sensing apparatus of Matsushima in view of Okino, because less time is devoted to exposure control activity than previously known readers or engines, and thereby have more time to spend on other reader control activities and the reader/engine can be constructed from simpler, less powerful and less costly electronic devices without adversely affecting its ability to successfully image an indicia under a wide variety of ambient illumination levels, and/or at a variety of different reading distances (Col. 2, lines 45 – 65 of Pettinelli).

As to claim 5, this claim differs from claim 1 only in that the limitation "a direct current offset controller" is additionally recited. The direct current offset controller is connected between the CCD and the variable control amplifier. The Matsushima reference teaches a clamp / CDS (7) which is connected to the output of the CCD (6) and the input of the auto-gain control (AGC (8)). Matsushima teaches a direct current offset controller (clamp / CDS 7) for controlling direct current offsets of output signals of the image sensor (CCD 6) under the control of an offset control signal (clamp level) (Para 29). Matsushima teaches that the clamp level can be changed by the microcomputer (16) (Para 29).

3. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima (US Patent Pub. # 2003/0016299) in view of

Okino (US Patent # 5,371,539), further in view of Pettinelli (US Patent # 6,254,003), and further in view of Shiga (US Patent Pub # 2005/0062874).

As to claim 3, Matsushima in view of Okino and further in view of Pettinelli teach the limitation "variable gain amplifier". Matsushima in view of Okino and further in view of Pettinelli do not teach a variable gain amplifier is a sample-and-hold amplifier architecture. Shiga (see fig. 1) teaches a variable gain amplifier (4) as a sample-and-hold amplifier architecture. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a variable gain amplifier with a sample-and-hold amplifier architecture taught by Shiga to the variable gain amplifier of Matsushima in view of Okino and further in view of Pettinelli, because the use of a sample and hold / gain control circuit is advantageous in that it does not give rise to such deterioration of a signal or decrease of the information amount of image data (Para 0105 of Shiga).

As to claim 7, this claim differs from claim 3 only in that the claim 3 depends on claim 1 whereas claim 7 depends on claim 5. Thus claim 7 is analyzed as previously discussed with respect to claim 3 above.

1. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima (US Patent Pub. # 2003/0016299) in view of Okino (US Patent # 5,371,539), further in view of Pettinelli (US Patent # 6,254,003), and further in view of Nagata (US Patent # 6,366,228).

As to claim 4, Matsushima in view of Okino and further in view of Pettinelli teach the limitation "A/D converter". Matsushima in view of Okino and further in view of Pettinelli do not teach an A/D converter is configured of a plurality of analog comparators. Nagata (see fig. 8) teaches an A/D converter configured of a plurality of analog comparators (CMP1 – 4) (Col. 12, lines 24 – 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided an A/D converter with a plurality of analog comparators taught by Nagata to the A/D converter of Matsushima in view of Okino and further in view of Pettinelli, because the use of analog comparators reduces the manufacturing cost and power (Col. 18, lines 43 - 55).

As to claim 8, this claim differs from claim 4 only in that the claim 4 depends on claim 1 whereas claim 8 depends on claim 5. Thus claim 8 is analyzed as previously discussed with respect to claim 4 above.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER K. PETERSON whose telephone number is (571)270-1704. The examiner can normally be reached on Monday - Friday 6:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran Sinh can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. K. P./
Examiner, Art Unit 2622
9/23/2009

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